4.2 A Serial-Link Transceiver with Transition Equalization

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One of the bottlenecks for increasing I/O data rates is the limited channel bandwidth. Channel equalization is used to compensate the low-pass characteristics. Area efficient multi-Gb/s equalizers have been implemented in both the transmitter and the receiver in the form of discrete-time FIR equalizers and DFEs. While these implementations have been effective in correcting the ISI at the sampling point, noise known as edge ISI is left or even injected on the transition edges. The resulting reduction in timing margin lowers the jitter tolerance and worsens BER. Some recent efforts have demonstrated equalization to cancel the edge ISI for relatively low-loss channels [1]. Edge equalization has also been applied to duo-binary signaling [2]. Recently, another technique was developed to equalize only at the edges [3]. The BER sensitivity to the edge ISI is substantially worse for heavily attenuated channels. This paper introduces both an FIR equalizer for data and edge pre-emphasis and a DFE that cancels edge ISI in the receiver. Moreover, we describe the noise and channel conditions needed for edge equalization to be effective.

Instead of using an FIR equalizer with a full bit-time delay chain (denoted DFIR) to cancel the edge ISI, one with a ($^1/_2$) bit-time delay chain is used (denoted XFIR). The XFIR equalizer creates the pulse response shown in Fig. 4.2.1 with half of the maximum amplitude at the data edges. By defining the edge samples in the XFIR equalizer, the timing margin is enlarged. However, the larger time opening is at the expense of the voltage opening and depends on the channel characteristics and random voltage/timing noise. By reducing the edge ISI, the XFIR equalizer is advantageous in systems with larger jitter. Figure 4.2.2(a) illustrates the tradeoff by indicating the point at which XFIR equalizer performance exceeds DFIR equalizer performance. Different channel bandwidths are represented by a normalized data sampling rate (f_{samp}/f_{-3dB}). For channels with more attenuation, the improvement in the timing is more substantial, causing an earlier crossover. Figure 4.2.2(a) also shows that using an XFIR equalizer is beneficial if the channel f_{-3dB} < data rate/12, for systems with 0.15 peak-to-peak unit-interval random jitter.

A direct implementation of the XFIR equalizer is to use $f_{clk} = 2f_{samp}$. However, substantially higher power is needed to support the high slew rates and larger number of flip-flops. Our design uses $f_{clk} = f_{samp}$ and latches as half-cycle delay elements. The latch outputs have half-cycle overlaps with adjacent taps, as shown in Fig. 4.2.2(b). Tap coefficients are adjusted such that the sum of the overlapping tap settings is the desired FIR weight. The proposed XFIR transmitter equalizer has 5 data taps and 5 edge taps. The delay chain is composed of CML latches and a CML XOR is used to create programmable inversions. The 10-tap driver is made of 7b current DACs for the first 4 taps and a 5b DAC for the remainder.

The XFIR transmitter equalizer is fabricated in 0.13µm CMOS and provides 250mV swing. Figure 4.2.3 shows the eye through a 120-inch FR4 channel that has f_{-3dB} of 70MHz and >30dB attenuation at 1.9GHz. At 3.8Gb/s, the DFIR equalizer opens the eye to (19.2mV and 198ps) and the XFIR equalizer opens it to (17mV and 212ps). Figure 4.2.3(c) shows the measured BER with a receiver sensitivity of 12mV. The receiver with an XFIR equalizer is error free (BER<1e-13) below 3.7Gb/s, but one with a DFIR equalizer needs <3.5Gbps for the same BER. The point at which an XFIR equalizer is no longer beneficial is not shown because the BER is too low to be measured. Simulations indicate that an XFIR equalizer becomes less efficient below 1Gb/s.

In a conventional DFE, data points are equalized, but the transition points are distorted by both ISI and the DFE feedback signals. The error introduces added noise to the CDR input. This paper proposes a DFE that subtracts the edge ISI (XDFE). As shown in Fig. 4.2.4, a normal DFE (DDFE) for equalizing data samples is in parallel to the added structure. Unlike the XFIR equalizer, the XDFE decouples the tradeoff between voltage and timing margins; therefore, the XDFE always results in a lower BER than the DDFE[1]. Since the XDFE cleans up the CDR input, the net impact depends on not only the channel attenuation and noise but also the CDR bandwidth. The drawback of the XDFE is that the timing margin of the data samples is not larger. By applying both the XFIR equalizer and XDFE, an optimum tradeoff can be reached.

A 3-tap half-rate DFE with first-tap look-ahead [4] is implemented in 0.18µm CMOS for both the XDFE and DDFE. For the feedback correction to be accurate, the tap current addition by the DFE must be fast, accurate, and linear. A large V_{gs} is used in the input differential pair for linearity. Cascode current sources are used for accurate current control. γ_1 is assumed to be negative, and the sign of $\gamma_{2,3}$ is achieved by switching the cascode bias through passgates. Sizing and layout of the differential pairs and PMOS loads minimize output parasitics.

The XDFE, receiving a 3.6Gb/s data stream without pre-emphasis, successfully equalizes 40-inch and 80-inch FR4 channels that have 250mV inputs as shown in Fig. 4.2.5. The data and edge eye diagrams are obtained by sweeping the voltage offset and phase of an auxiliary sampler in parallel with the receiver. The auxiliary sampler is an exact copy of the data sampler, and it is also used to detect the signal amplitude during equalizer adaptation. In Fig. 4.4.5(e), the XDFE cancels the ISI, and thus the transitions are better defined than in the DDFE in Fig. 4.2.5(d). The recovered clock jitter is an indication of the XDFE performance. Measurement shows a reduction from 31.1ps$_{pp}$ to 28.9ps$_{pp}$.

Instead of equalizing the input of the CDR circuit, designers have applied digital edge filtering at the expense of lower CDR-loop bandwidths [2]. For instance, edge filtering can remove the edges with worse slew rates and their associated ISI. The result is a cleaner CDR output. Measurement of our reconfigured test-chip shows a jitter of 26.7ps$_{pp}$. The XDFE can still be applied to remove residual ISI from highly-attenuating channels. Jitter is further improved to 25.5ps$_{pp}$. To achieve this improved performance without XDFE, a substantially greater amount of filtering would be needed. One can consider the XDFE as a means to improve jitter tolerance. As shown in Fig. 4.2.6(b), the BER is measured with different CDR update rates. For a given BER (1e-7), an XDFE can operate at 1.5× higher update rate than a DDFE alone.

The transmitter consumes 137mW and the receiver with eye monitor circuits and CDR consumes 45mW from simulations.

Acknowledgment:
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References:
[1] J. Buckwalter et al., "A 10Gb/s Data-Dependent Jitter Equalizer," *CICC*, pp. 39-42, Oct., 2004.
[2] K. Yamaguchi et al., "12Gb/s Duobinary Signaling with x2 Oversampled Edge Equalization," *IEEE ISSCC Dig. Tech. Papers*, pp 68-69, Feb., 2005.
[3] B Brunn, "Edge Equalization NRZ," http://www.ieee802.org/3/ap/public/jul04/brunn_01_0704.pdf, July, 2004.
[4] R.S Kajley et al., "A Mixed-Signal Decision-Feedback Equalizer that uses a Look-Ahead Architecture," *IEEE J. Solid-State Circuits*, pp.450-459, Mar., 1997.

[1]A double rate DFE to correct for the transitions is theoretically feasible but not practical due to the feedback delay. The result would also be very

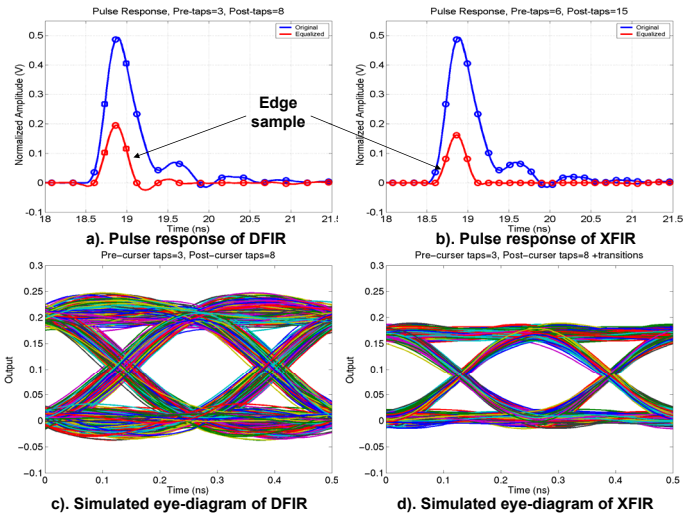


Figure 4.2.1: Simulated pulse responses and eye diagrams for DFIR and XFIR.

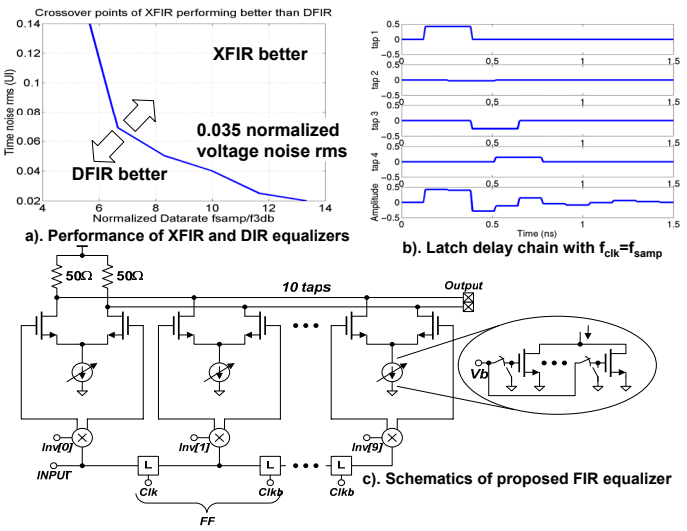


Figure 4.2.2: Schematics and performance of FIR equalizer.

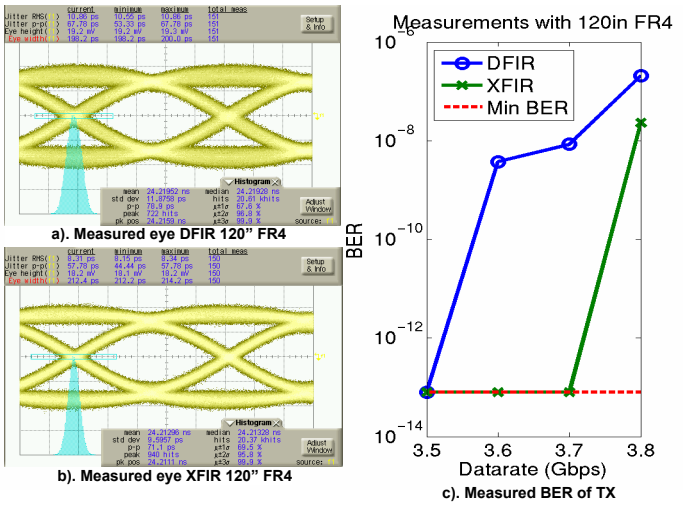


Figure 4.2.3: Measurement results for TX.

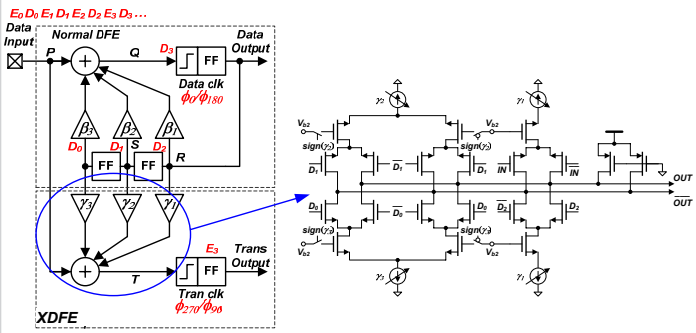


Figure 4.2.4: XDFE schematic.

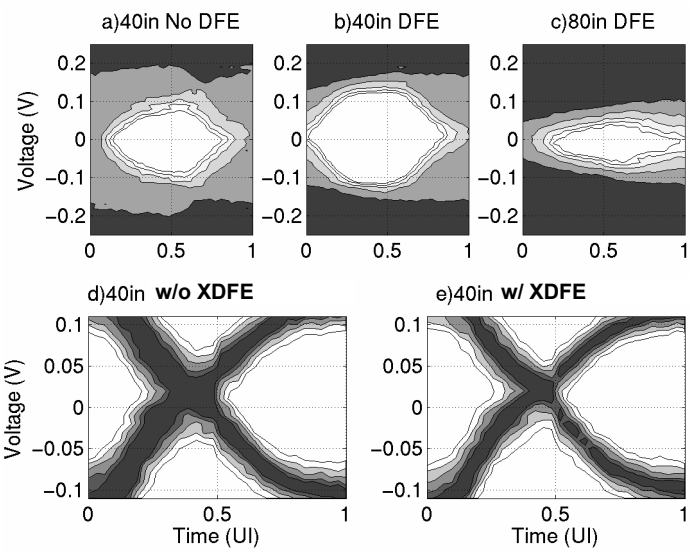
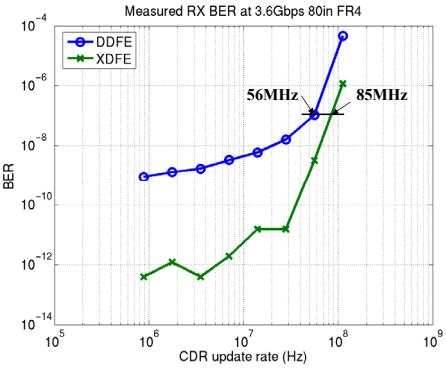


Figure 4.2.5: Data eye-diagram of DDFE and edge-diagram of XDFE.

	DDFE	XDFE
w/o edge filtering	31.11ps	28.89ps
w/ edge filtering	26.67ps	25.56ps

a). Jitter (p2p) of different architecture of DFE



b). Measured BER of RX

Figure 4.2.6: Measurement results for the receiver.

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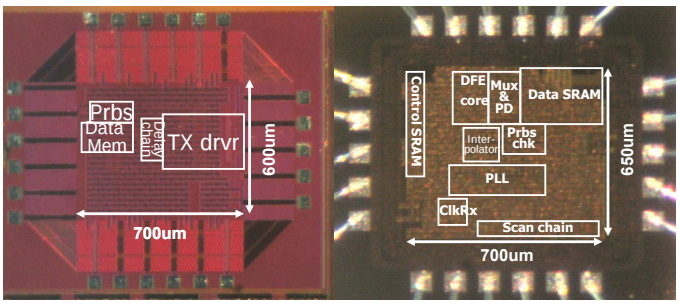

a). TX in 0.13-µm CMOS

b). RX in 0.18-µm CMOS

Figure 4.2.7: Die photo.

